CLAIMS

What is claimed is:

1. A method, comprising:

receiving a plurality of bytes in a first buffer having a size with a number of the plurality of bytes containing data;

determining a state of the plurality of bytes by a controller at least one clock cycle before a rotation of the plurality of bytes; and

predicting a rotation amount for the rotation of the plurality of bytes in a rotator based on the state.

2. The method of claim 1, wherein the rotation amount is predicted to be the size minus the number when the controller determines that a buffer, coupled to receive the plurality of bytes from the rotator, is empty.

3. The method of claim 1, wherein the rotation amount is predicted to be the size minus the number when the controller determines that a buffer, coupled to output the plurality of bytes to the rotator, contains a start of packet signal.

4. The method of claim 1, wherein the rotation amount is predicted to be the size minus the number when the first buffer contains a start of packet signal, the buffer coupled to output the number of bytes to the rotator.

5. The method of claim 1, wherein the first buffer is coupled to output the plurality of bytes to the rotator and a second buffer is coupled to

receive the plurality of bytes from the rotator, and wherein the rotation amount is predicted to be zero when all of the plurality of bytes in the first buffer are written to the second buffer.

6. The method of claim 1, wherein the first buffer is coupled to output the plurality of bytes to the rotator and a second buffer is coupled to receive the plurality of bytes from the rotator, and wherein the rotation amount is predicted to be zero when the first buffer contains an end of packet signal and a number of bytes in the first and second buffers is less than the size.

7. The method of claim 1, wherein the first buffer is coupled to output the plurality of bytes to the rotator and a second buffer is coupled to receive the plurality of bytes from the rotator, and wherein the rotation amount is predicted to be twice the size minus the number of bytes in the first and second buffers when a number of bytes in the first buffer and second buffers exceeds the size.

8. An apparatus, comprising:

means for receiving a plurality of bytes having a size;

means for determining a state of the plurality of bytes at least one clock cycle before a rotation of the plurality of bytes; and

means for predicting a rotation amount for the rotation of the plurality of bytes based on the state.

9. The apparatus of claim 8, further comprising means for rotating the plurality of bytes based on the state.

10. The apparatus of claim 9, wherein the means for rotating comprises:

a rotation circuit coupled to receive an input and generate an output; and

a multiplexer coupled to receive the input and the output of the rotation circuit, the multiplexer to select between the input and the output based on a rotate amount control signal.

11. A method, comprising:

predicting a first number of bytes residing in a first buffer in a succeeding clock cycle; and

performing a calculation of a rotation amount of a second number of bytes received from a second buffer based on the prediction, the calculation performed in a current clock cycle.

12. The method of claim 11, wherein the first number is predicted to be zero.

13. The method of claim 12, wherein the first buffer is empty.

14. The method of claim 12, wherein the second buffer contains a start of packet signal.

15. The method of claim 12, wherein all of the second number of bytes are written to the first buffer.

16. The method of claim 11, wherein the first and second buffers have a size and wherein the first number is predicted to be the size minus the

number of bytes in the second buffer when the second buffer contains a start of packet signal.

17. The method of claim 11, wherein the first number is predicted to be twice the size minus a total number of bytes in the first and second buffers when the total number of bytes in the first buffer and second buffers exceeds the size.

18. The method of claim 16, wherein the size is 16.

19. A data aligner, comprising:

a first buffer coupled to receive a clock signal have a plurality of clock cycles;

a controller; and

a rotator coupled to the controller and the first buffer, the rotator comprising:

a first rotation circuit coupled to receive an input and generate a first output; and

a first multiplexer coupled to receive the input and the first output of the rotation circuit, the first multiplexer to select between the input and the first output based on a first rotate amount control signal receive from the controller, the first rotate amount control signal determined by predicting a number of bytes residing in the first buffer in a succeeding clock cycle.

20. The data aligner of claim 19, wherein the first buffer comprises a control section coupled to receive a buffer control signal from the controller.

21. The data aligner of claim 19, further comprising a second buffer coupled to the rotator, wherein the input is received from the second buffer.

22. The data aligner of claim 19, wherein the rotator further comprises:

a second rotation circuit coupled to receive an output of the first multiplexer and generate a second output; and

a second multiplexer coupled to receive the second output of the second rotation circuit and the output of the first multiplexer, the second multiplexer to select between the second output and the output of the first multiplexer based on a second rotate amount control signal receive from the controller, the second rotate amount control signal determined by predicting the number of bytes residing in the first buffer in the succeeding clock cycle.